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10/569,530	02/24/2006	Sturla Lutnaes	956315	6019

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EXAMINER	
SHOLEMAN, ABU S	
ART UNIT	PAPER NUMBER
2437	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/569,530	LUTNAES, STURLA	
	Examiner	Art Unit	
	ABU SHOLEMAN	2437	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/24/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 of the instant application filed on 02/24/2006 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5, 9, 11, 16-17,19, 21, and 25-27 are rejected under 35 U.S.C.103 (a) as being unpatentable over Turkboylari (20030140238) (hereinafter Turkboylari) in view of Schu et al (5973968) (hereinafter Schu).

As per claim 1, Turkboylari discloses

"copying security data from the non-volatile memory to the working memory, wherein the security data is to be write-protected" as (**on page 3, [0026], "boot loader sequence typically loads user code from non-volatile memory to into RAM", user code can view as a security data and this data is write protected by a write-protection function**);

"activating a blocking function for the security data in the working memory, wherein activating is triggered by the copying being made to the working memory" as (**on page 3, [0026], "security logic ensures that the authenticated code is not further altered after it has been loaded into system RAM" when code is loaded into RAM then write -protection function get activated for blocking any alteration into a portion of volatile memory RAM**);

"monitoring all communication with the working memory" as (**on page 3, [0026], security logic ensures (i.e. monitoring) that there is not any alteration after upload any code in RAM**);

"blocking all write attempts to the copied security data stored in the working memory according to the blocking function, wherein at least activating a blocking function" as (**on page 3, [0026], "security logic ensures that the authenticated code is not further altered after it has been loaded into system RAM" when code is loaded into RAM then write -protection function get activated for blocking any alteration into a portion of volatile memory RAM and , write-protection function is a blocking function and system security is maintained by ensuring that security-sensitive data and code are protect by write-protected function when authentication code for secure applications to be loaded into RAM upon reset or power-up**) ,

Turkboylari discloses monitoring communication and blocking write attempts performed but fails to disclose " independently of a central processing unit of the

electronic data processing device, such that the central processing unit cannot manipulate the security data".

However, Schu discloses “monitoring communication and blocking write attempts performed independently of a central processing unit of the electronic data processing device, such that the central processing unit cannot manipulate the security data” as (**on page 9, lines 55-67, and Fig .3, In response to write signal 210b, write lock logic is applied 230 by logic circuitry 208 in order to verify the appropriateness of providing write access to write lock RAM 206. If, after application of the write lock logic 230, write access to write lock RAM 206 is authorized 232, data is written 234 to the appropriate address locations in write lock RAM 206. If write lock logic circuitry 208 determines that write access to write lock RAM 206 is not authorized 232, write lock logic circuitry 208 prevents write signal 210b from effecting write access to write lock RAM 206. A memory fault condition typically arises upon failure to authorize write access to write lock RAM 206 in response to an errant write signal 210b generated by processor 202 or other direct memory addressing component. The fault condition is typically indicated in system memory by a latched fault bit or byte in a fault status register of processor 202, Write lock logic circuitry 208 is independent from processor 202. Any write signal 210b is coming from processor to write in write locked RAM 206 is blocked by write lock logic circuitry 208. CPU gets blocked by write lock logic circuitry while trying to write in locked RAM**).

Since Schu' invention provided an independent write lock logic circuitry to block write attempt to write locked RAM, it would have been obvious to one skill in the art to utilize Schu's method in Turkboylari's invention in the manner discussed because doing so would be nothing more than applying a known technique to a known method ready for improvement to yield predictable results. In this case the predictable result would improve CPU's performance while protecting authentication code.

As per claim 3, Turkboylari in view of Schu disclose all the limitations set forth above, " copying data comprises copying only the security data from the non-volatile memory to the working memory independently of the central processing unit of the data processing device and coping any further data under the control of the central processing unit of the device" as (Turkboylari, **on page 3, [0026], "boot loader sequence typically loads user code from non-volatile memory to into RAM", user code can view as a security data and this data is write protected by a write-protection function.** Schu, Fig.3, write signal 210a can write data on RAM and write signal 210b can write data in locked RAM without processor 202 supervision).

As per claim 5, Turkboylari in view of Schu disclose copying comprises copying all data from the non-volatile memory to the working memory under the control of the central processing unit of the device" as (**Turkboylari, on page 3, [0026], loads user code from non-volatile memory to RAM and Schu, Fig 3, write signal 210a writes into RAM 204. it does not write in write locked RAM 206**).

As per claim 9, this claim is directed to a device and contains limitations that are substantially similar to those recited in claim 1 above, and accordingly is rejected for similar reasons.

As per claim 11, this claim is directed to a device and contains limitations that are substantially similar to those recited in claim 3 above, and accordingly is rejected for similar reasons.

As per claim 16, Turkboylari in view of Schu disclose wherein it is implemented in hardware as (Turkboylari, Fig. 1 and Schu, Fig. 3).

As per claim 17, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 1 above, and accordingly is rejected for similar reasons.

As per claim 19, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 3 above, and accordingly is rejected for similar reasons.

As per claim 21, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 5 above, and accordingly is rejected for similar reasons.

As per claim 25, Turkboylari in view of Schu discloses “wherein the device for blocking write attempts is implemented in hardware” as (Turkboylari, Fig. 1 and Schu, Fig. 3).

As per claim 26, Turkboylari in view of Schu disclose "wherein the device is a portable communication device" as (Turkboylari, [0005]).

As per claim 27, Turkboylari in view of Schu disclose "wherein the device is a cellular phone" as (Turkboylari, [0005]).

4. Claims 2, 4, 6, 10, 12, 13, 18, 20, and 22 are rejected under 35 U.S.C.103 (a) as being unpatentable over Turkboylari (20030140238) (hereinafter Turkboylari) in view of Schu et al (5973968) (hereinafter Schu) and further in view of Lasker et al (5586291) (hereinafter Lasker).

As per claim 2, Turkboylari in view of Schu disclose all the limitations set forth above, Turkboylari discloses "wherein an area of the security data in the non-volatile memory is pre-stored in a device for blocking write attempts and used at lest in relation to activating a blocking function". But fails to disclose " wherein an area of the security data in the non-volatile memory is pre-defined in a device for blocking write attempts and used at lest in relation to activating a blocking function.

However, Lasker discloses wherein an area of the security data in the non-volatile memory is pre-defined in a device as (**on page 4, lines 5-12, and the controller microprocessor allocates a predetermined number of memory blocks in the non-volatile cache memory modules. After allocating the memory blocks of the non-volatile cache memory, the disk controller selects and allocates a**

corresponding plurality of memory blocks in the volatile memory modules. Host supplied write-data is then stored in the allocated memory blocks of the non-volatile memory module and The cache memory control circuit then performs a direct memory access (DMA) operation to copy the write-data from the allocated memory blocks of the non-volatile memory module to the corresponding allocated memory blocks of the volatile memory module).

Therefore, It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to modify the teaching of Turkboylari in view of Schu by including a predetermined number of memory blocks in ROM that is taught by Lasker because it would provide a higher efficiency for data storage in volatile memory.

As per claim 4, Turkboylari in view of Schu disclose all the limitations set forth above. Turkboylari discloses “wherein an area of the security data in the non-volatile memory and an area for storage of the security data in the working memory are copied and wherein activating a blocking function is triggered by the copying being made to the pre-defined area in the working memory and the blocking function is activated for that area of the working memory". But Turkboylari fails to disclose wherein an area of the security data in the non-volatile memory and an area for storage of the security data in the working memory are predefined’.

However, Lasker discloses wherein an area of the security data in the non-volatile memory and an area for storage of the security data in the working memory are

predefined as (**on page 4, lines 5-12, and the controller microprocessor allocates a predetermined number of memory blocks in the non-volatile cache memory modules. After allocating the memory blocks of the non-volatile cache memory, the disk controller selects and allocates a corresponding plurality of memory blocks in the volatile memory modules. Host supplied write-data is then stored in the allocated memory blocks of the non-volatile memory module and The cache memory control circuit then performs a direct memory access (DMA) operation to copy the write-data from the allocated memory blocks of the non-volatile memory module to the corresponding allocated memory blocks of the volatile memory module**).

Therefore, It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to modify the teaching of Turkboylari in view of Schu by including a predetermined number of memory blocks in ROM and RAM that is taught by Lasker because it would provide a higher efficiency for data storage in volatile memory.

AS per claim 6, Turkboylari in view of Schu disclose all the limitations set forth above, Turkboylari in view of Schu disclose " wherein an area of the security data in the non –volatile memory and wherein activating a blocking function is triggered by a first detection of copying of security data in the non-volatile memory to an area of the working memory and blocking function is activated for that area of the working

memory" , but fails to disclose "wherein an area of the security data in the non-volatile memory is pre-defined area".

However, Lasker disclose "wherein an area of the security data in the non-volatile memory is pre-defined area" as (**on page 4, lines 5-12, and the controller microprocessor allocates a predetermined number of memory blocks in the non-volatile cache memory modules. After allocating the memory blocks of the non-volatile cache memory, the disk controller selects and allocates a corresponding plurality of memory blocks in the volatile memory modules. Host supplied write-data is then stored in the allocated memory blocks of the non-volatile memory module and The cache memory control circuit then performs a direct memory access (DMA) operation to copy the write-data from the allocated memory blocks of the non-volatile memory module to the corresponding allocated memory blocks of the volatile memory module**).

Therefore, It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to modify the teaching of Turkboylari in view of Schu by including a predetermined number of memory blocks in ROM and RAM that is taught by Lasker because it would provide a higher efficiency for data storage in volatile memory.

As per claim 10, this claim is directed to a device and contains limitations that are substantially similar to those recited in claim 2 above, and accordingly is rejected for similar reasons.

As per claim 12, this claim is directed to a device and contains limitations that are substantially similar to those recited in claim 4 above, and accordingly is rejected for similar reasons.

As per claim 13, this claim is directed to a device and contains limitations that are substantially similar to those recited in claim 6 above, and accordingly is rejected for similar reasons.

As per claim 18, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 2 above, and accordingly is rejected for similar reasons.

As per claim 20, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 4 above, and accordingly is rejected for similar reasons.

As per claim 22, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 6 above, and accordingly is rejected for similar reasons.

5. Claims 7, 14 and 23 are rejected under 35 U.S.C.103 (a) as being unpatentable over Turkboylari (20030140238) (hereinafter Turkboylari) in view of Schu et al (5973968) (hereinafter Schu) and further in view of Porter et al (US2003/0226029) (hereinafter Porter).

As per claim 7, Turkboylari in view of Schu disclose all the limitations set forth above, but fail to disclose "wherein the blocking function comprises changing the destination address of the data transferred to the working memory".

However, Porter disclose "changing the destination address of the data transferred to the working memory" as (**on page 5, [0039], Memory controllers are used to store data in memory and [0040] It can be used to change the address in which data is stored in memory and memory controller can change**).

Therefore, It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to modify the teaching of Turkboylari in view of Schu's write-protected function by including a memory controller that is taught by Porter because it would provide a higher protection for security-sensitive data or code while uploading in RAM.

As per claim 14, this claim is directed to a device and contains limitations that are substantially similar to those recited in claim 7 above, and accordingly is rejected for similar reasons.

As per claim 23, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 7 above, and accordingly is rejected for similar reasons.

6. Claims 8, 15 and 24 are rejected under 35 U.S.C.103 (a) as being unpatentable over Turkboylari (20030140238) (hereinafter Turkboylari) in view of Schu et al (5973968) (hereinafter Schu) and further in view of Anderson (6115819)(hereinafter Anderson).

As per claim 8, Turkboylari in view of Schu disclose all the limitations set forth above, but fail to disclose "Disconnecting a debugging unit at least when copying the security data to the working memory and reconnect the debugging unit when the blocking function has been activated".

However, Anderson discloses “Disconnecting a debugging unit at least when copying the security data to the working memory and reconnect the debugging unit when the blocking function has been activated’ as (**on page 6, lines 45-48, The AM will allow or disallow the access by controlling gate 44 to pass or not pass the read or write command in the RAM, controlling gate 44 can be view as a debugging unit. On page 4, lines 60-65, access monitor decides that the**

transaction is not permitted then it can disable the date through which the data transfer would occur).

Therefore, It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to modify the teaching of Turkboylari in view of Schu by including The AM that is controlling gate that is taught by Anderson because it would provide a higher protection for security-sensitive data or code while uploading in RAM.

As per claim 15, this claim is directed to a device and contains limitations that are substantially similar to those recited in claim 8 above, and accordingly is rejected for similar reasons.

As per claim 24, this claim is directed to an electronic data processing device and contains limitations that are substantially similar to those recited in claim 8 above, and accordingly is rejected for similar reasons.

Examiner Notes

7. Examiner cites particular columns and line numbers in the references as applied to the claims below for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the

references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

8. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05(c).

9. The following reference teaches execution of trial data.

US 20030140238

US 5973968

US 5586291

US 6078520

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abu Sholeman whose telephone number is (571)270-7314. The examiner can normally be reached on Monday through Thursday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 30, 2009

Abu Sholeman
Examiner
Art unit 2437

/Emmanuel L. Moise/
Supervisory Patent Examiner, Art Unit 2437